

7. The method of yield improvement of VLSI integrated circuits according to claim 6 in which steps c) through e) are repeated in the loop until either geometry distortions of all correction segments meet the minimum requirements determined in step d) of claim 1 or preset number of iterations is exceeded.

Abstract

A method for performing self-consistent minimization of IC design and process interactions is disclosed. This method is based on calculating the amount of design-process interaction based on the information derived from circuit sensitivity analysis and process characterization. Optical proximity correction is subsequently performed in such a way that a) ensures that desired circuit performance is achieved in a given manufacturing environment if at all possible and b) also limits the increase in mask complexity to a realistic minimum.